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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,011	09/11/2003	Dong-Hyuk Ju	AMD-H0558	8590
7590 09/07/2005 WAGNER, MURABITO & HAO LLP Two North Market Street, Third Floor San Jose, CA 95113			EXAMINER LEE, CHEUNG	
			ART UNIT 2812	PAPER NUMBER
DATE MAILED: 09/07/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,011	JU, DONG-HYUK	
	Examiner	Art Unit	
	Cheung Lee	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:
 - a. On page 8, line 22, the figure number "6" does not exist, it needs to be corrected to "6A".
 - b. On page 8, line 23, the word "date" is not appropriate, it needs to be changed to "gate".
 - c. On page 9, lines 9, 10, and 11, the step number "610" does not exist, it needs to be corrected to "510".
 - d. On page 9, line 14, the step number "620" does not exist, it needs to be corrected to "520".
 - e. On page 10, line 1, the figure number "6" does not exist, it needs to be corrected to "6C".
 - f. On page 10, line 18, the figure number "6" does not exist, it needs to be corrected to "6D".
 - g. On page 13, line 14, the figure number "6" does not exist, it needs to be corrected to "6C".

Claim Objections

2. Claims 1, 8, and 13 are objected to because of the following informalities:
 - a. In claim 1, line 3, insert --first-- before "annealing" for clarity of the claim.

- b. In claim 8, lines 2 and 4, insert --first-- and --second-- respectively before "dopant" for clarity of the claim.
- c. In claim 13, lines 2 and 4, insert --first-- and --second-- respectively before "dopant" for clarity of the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

- 3. Claims 1-3, 8-10, and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu (U.S. Publication 2002/0102793).
- 4. With respect to claim 1, Wu discloses a method for fabricating a memory device (page 2, paragraph 12) comprising: depositing a dopant in a first region of a semiconductor substrate of a memory device (page 4, paragraph 26; page 5, paragraph 29); performing an annealing process upon said semiconductor substrate (page 5, paragraph 29); performing a second depositing of a dopant in a second region of said semiconductor substrate (page 4, paragraph 26; page 5, paragraph 29); and performing a second annealing process upon said semiconductor substrate (page 5, paragraph 30).
- 5. With respect to claim 8, Wu discloses a method for fabricating a flash memory device (page 2, paragraph 12) comprising: performing a partial annealing process (page

5, paragraph 29) upon a dopant deposited in a first region of a semiconductor substrate of said flash memory device (page 4, paragraph 26; page 5, paragraph 29); depositing a dopant in a second region of said semiconductor substrate (page 4, paragraph 26; page 5, paragraph 29); and performing a second annealing process (page 5, paragraphs 30-31) wherein said dopant deposited in said first region and said dopant deposited in said second region are simultaneously annealed. The examiner interpreted the annealing process performed after the impurities implantation (page 5, paragraph 29) to be a partial annealing process because additional thermal treatments (page 5, paragraphs 30-31) inherently further the initial annealing.

6. With respect to claim 13, Wu discloses a method for fabricating a memory device (page 2, paragraph 12) comprising: initiating a partial diffusion of a dopant deposited in a first region of a semiconductor substrate of a memory device (page 4, paragraph 26; page 5, paragraph 29); depositing a dopant in a second region of said semiconductor substrate (page 4, paragraph 26; page 5, paragraph 29); and initiating a second diffusion (page 5, paragraphs 30-31). The examiner interpreted that the rapid thermal annealing and the reflow inherently further diffuse the dopant in said first region concurrently with the diffusion of the dopant in said second region.

7. With respect to claims 2 and 14, Wu discloses a method for fabricating a memory device as set forth in claims 1 and 13, wherein said depositing a dopant (page 4, paragraph 26; page 5, paragraph 29) comprises creating an impurity concentration in a semiconductor substrate (page 4, paragraph 26) of a flash memory device (page 2, paragraph 12).

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8. With respect to claim 3, Wu discloses a method for fabricating a memory device as set forth in claim 1, wherein said depositing a dopant (page 4, paragraph 26; page 5, paragraph 29) comprises depositing a dopant for a plurality of semiconductor devices (fig. 5B) in a periphery region of said memory device (fig. 5B, regions 21b and 21c).

9. With respect to claim 4, Wu discloses a method for fabricating a memory device as set forth in claim 3, wherein said performing a second depositing (page 4, paragraph 26; page 5, paragraph 29) comprises depositing a dopant for a plurality of memory cells (fig. 5B) in a core region of said semiconductor substrate of said memory device (fig. 5B, region 21a).

10. With respect to claims 9 and 15, Wu discloses a method for fabricating a memory device as set forth in claims 8 and 13, wherein said first region (fig. 5B, regions 21b and 21c) comprises a plurality of semiconductor devices disposed in a periphery region (fig. 5B, regions 21b and 21c) of said flash memory device (page 3, paragraph 20; page 5, paragraph 32) and comprising performing a partial annealing process (page 5, paragraph 29) upon said plurality of semiconductor devices (fig. 5B). The examiner interpretation concerning partial annealing process stated in claim 8 also applies.

11. With respect to claims 10 and 16, Wu discloses a method for fabricating a memory device as set forth in claims 9 and 15, wherein said second region (fig. 5B, region 21a) comprises a plurality of memory cells disposed in a core region (fig. 5B, region 21a) of said flash memory device (page 3, paragraph 20; page 5, paragraph 32) and comprising performing a partial annealing process (page 5, paragraph 29) upon

said plurality of memory cells (fig. 5B). The examiner interpretation concerning partial annealing process stated in claim 8 also applies.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 5-7, 11-12, and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu.

13. With respect to claim 5, Wu discloses a method for fabricating a memory device as set forth in claims 4, but Wu does not disclose expressly wherein a plurality of parameters of said second annealing process (page 5, paragraphs 30-31) are selected based upon an electrical characteristic of said plurality of memory cells (fig. 5B). Wu discloses a titanium metal deposition and then performs annealing process (page 5, paragraph 30), and the parameters for annealing process are based to form the titanium-disilicide layer of the memory cells. So, it is obvious that the second annealing process parameters are selected based upon electrical characteristic of memory cells.

14. With respect to claim 6, Wu discloses a method for fabricating a memory device as set forth in claim 5, wherein said annealing process and said second annealing process (page 5, paragraphs 29-31) comprise a cumulative annealing process for said

plurality of semiconductor devices (fig. 5B). The examiner interpreted the reflow process at 850°C inherently increase^d annealing time to cumulatively anneal the device.

15. With respect to claim 7, Wu discloses a method for fabricating a memory device as set forth in claim 6, but Wu does not disclose expressly wherein a plurality of parameters of said cumulative annealing process (page 5, paragraphs 29-31) are selected based upon an electrical characteristic of said plurality of semiconductor devices (fig. 5B). The examiner interpretation concerning cumulative annealing process stated in claim 6, and the arguments concerning annealing process parameters stated in claim 5 also apply.

16. With respect to claim 11, Wu discloses a method for fabricating a memory device as set forth in claim 10, but Wu does not disclose expressly wherein a plurality of parameters of said second annealing process (page 5, paragraphs 30-31) are selected based upon an electrical characteristic of said plurality of memory cells (fig. 5B). The arguments concerning annealing process parameters stated in claim 5 also apply.

17. With respect to claim 12, Wu discloses a method for fabricating a memory device as set forth in claim 11, but Wu does not disclose expressly wherein a plurality of parameters of said partial annealing process (page 5, paragraph 29) are selected based upon an electrical characteristic of said plurality of semiconductor devices (fig. 5B) and upon said plurality of parameters of said second annealing process (page 5, paragraphs 30-31). The arguments concerning annealing process parameters stated in claim 5 also apply.

18. With respect to claim 17, Wu discloses a method for fabricating a memory device as set forth in claim 16, but Wu does not disclose expressly wherein a plurality of parameters of said second diffusion (page 5, paragraphs 29-31) are selected based upon an electrical characteristic of said plurality of memory cells (fig. 5B). The examiner interpretation concerning diffusing process stated in claim 13 and the arguments concerning annealing process parameters stated in claim 5 also apply.

19. With respect to claim 18, Wu discloses a method for fabricating a memory device as set forth in claim 17, but Wu does not disclose expressly wherein said partial diffusion and said second diffusion (page 5, paragraphs 29-31) comprise a cumulative diffusion for said plurality of semiconductor devices (fig. 5B). The examiner interpretation concerning diffusing process stated in claim 13 also applies. And it is obvious that the annealing steps accumulate to finish diffusing as claimed limitation.

20. With respect to claim 19, Wu discloses a method for fabricating a memory device as set forth in claim 18, but Wu does not disclose expressly wherein a plurality of parameters of said cumulative diffusion (page 5, paragraphs 29-31) are selected based upon an electrical characteristic of said plurality of semiconductor devices (fig. 5B). The examiner interpretation concerning diffusing process stated in claim 13 and the arguments concerning annealing process parameters stated in claim 5 also apply.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheung Lee whose telephone number is 571-272-5977.

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The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cheung Lee

August 25, 2005



HA NGUYEN
PRIMARY EXAMINER